5.3: Analytic Models of Synchronized Dual-Gate a-IGZO TFTs

Gwanghyeon Baek and Jerzy Kanicki
Department of Electrical Engineering and Computer Science
University of Michigan, Ann Arbor, MI, U.S.A. 48109
kanicki@eecs.umich.edu

Abstract: *The equations for the transfer characteristics and sub-threshold swing of dual-gate a-IGZO TFTs, when the top and bottom gate electrodes are connected (synchronized), are developed based on device physics. From these equations, it is found that synchronized DG a-IGZO TFTs can be considered as conventional TFTs with modified gate capacitance and threshold voltage. The device parameters of coplanar homojunction DG TFTs are extracted using these equations.*

Keywords: dual-gate; thin film transistor; a-IGZO; transfer characteristic; sub-threshold swing

Introduction

There has been an increased interest in adapting amorphous Indium–Gallium–Zinc–Oxide (a-IGZO) thin film transistors (TFTs) as next generation TFT technology for active matrix flat-panel displays.[1, 2] The a-IGZO TFTs have a field-effect mobility (μ) ranging from 8 to 20 cm^2/V s, a sub-threshold swing (SS) below 200 mV/dec, a threshold voltage (V_{TH}) around 0 V, and an off-current below 1×10^{-12} Ampere.[3] Much of the research effort has been focused on improving the a-IGZO material properties as well as gate dielectric interface.[4, 5] However, it is important to keep in mind that the performance of TFTs is also influenced by the device structure.

A dual-gate (DG) a-IGZO TFT structure has both a bottom gate (BG) and a top gate (TG) electrodes.[6-8] It is well known that the electrical performance of DG TFTs is improved because a larger portion of the channel area is controlled by an additional gate electrode. Furthermore, it is found that DG a-IGZO TFTs have higher stabilities under light illumination. To understand the operation principle of DG a-IGZO TFTs, the mathematical analysis based on device physics should be investigated. Abe *et.al.* described the mathematical analysis of DG a-IGZO TFTs when either TG or BG bias is constant.[9] In this paper, as an extension work of the previous Abe's work, we analyzed a-IGZO DG TFTs when both TG and BG are tied together (synchronized). In the latter part of this paper, the TFT parameters of the DG a-IGZO coplanar homo-junction TFT are extracted using the proposed models.

TFT Modeling

Figure 1 shows a schematic cross section of a DG TFT with a channel length, L. The mathematical derivation is based on the following assumptions.

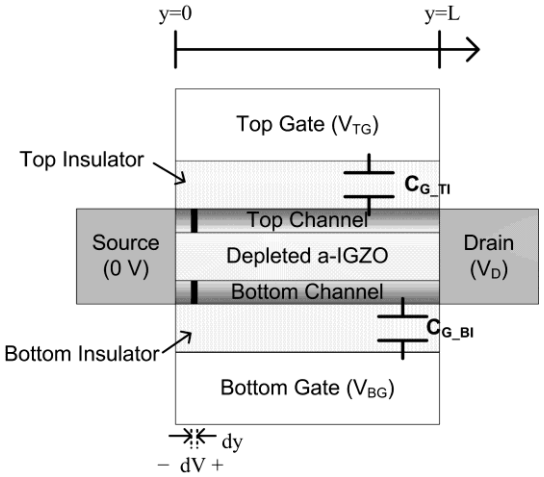

Figure 1. Schematic cross-section of a DG TFT

- (*Constant Mobility*) The mobility is constant during TFT operations.
- (*Gradual Channel*) The voltages vary gradually along the channel from the source to the drain
- (*Two-Dimension*) The TFT is two-dimensional; The TFT does not have the channel width (W) dependency
- (*DC Measurement*s) The bias voltage or current can be changed only after the TFT is under equilibrium states.
- (*Long Channel*) There is no interaction between the source/drain electrodes.

The above assumptions could often fail for the field effect transistors (FETs), such as a-IGZO TFTs. However, we believe that the model using these assumptions can successfully explain the characteristics of conventional TFT parameters, such as μ, V_{TH}, and SS. The similar assumptions are also employed in the SPICE Level 1 model for the FETs.[10]

On Operation Region: The surface charge density, Q_S, can be written is the sum of bottom and top surface charge density. (Q_{BS} and Q_{TS}, respectively)

$$Q_s = Q_{BS} + Q_{TS} \tag{1}$$

From the parallel plate capacitor model;

$$Q = CV \tag{2}$$

Therefore, the Q_S can be written as

$$Q_s = C_{BI}\left(V_{BG} - V_{BTH0} - V(y)\right) + C_{TI}\left(V_{TG} - V_{TTH0} - V(y)\right) \tag{3}$$

where C_{BI} and C_{TI} are the capacitances per unit area of the bottom and top insulators, respectively. V(y) is the channel voltage at the position y, in the horizontal direction along the channel length from the source to drain. V_{BTH0} and V_{TTH0} correspond to the threshold voltages of the single gate TFT only with the bottom or the top gate electrode, respectively. The voltage drop, dV, between y to y+dy is given by [11]

$$dV = \frac{I_D dy}{W\mu|Q_s|} \tag{4}$$

By integrating the Eq. (4) for entire channel length (from y = 0 to L). Over the length of the channel, the channel voltage varies gradually from the source voltage V(0) = 0V to the drain voltage V(L) = V_D. The drain current (I_D) of the DG TFT is given by Eq. (5). Since V_G=V_{BG}=V_{TG}, in synchronized DG operation, Eq(5) is simplified into Eq. (6).

For more simplification, we define the dual gate capacitances per unit area (C_{DI}) and the threshold voltage of synchronized DG operation (V_{DTH})

$$C_{DI} = C_{BI} + C_{TI} \tag{7}$$

$$V_{DTH} = \frac{C_{BI}V_{BTH0} + C_{TI}V_{TTH0}}{C_{DI}} \tag{8}$$

Then, I_D can be expressed as

$$I_D = \frac{W}{L}\mu C_{DI}\frac{\{V_G - V_{DTH}\}^2}{2}\left[1 - \left\{1 - \frac{V_D}{V_G - V_{DTH}}\right\}^2\right] \tag{9}$$

If the TFT is under linear operation region, $V_G - V_{DTH} \gg V_D$, Eq 9 can be approximated into

$$I_D = \frac{W}{L}\mu C_{DI}(V_G - V_{DTH})V_D \tag{10}$$

Moreover, in saturation operation region, $V_G - V_{DTH} \ll (C_{DI}/C_{BI})V_D$,

$$I_D = \frac{W}{2L}\mu C_{DI}(V_G - V_{DTH})^2 \tag{11}$$

Sub-threshold Region: In order to calculate the I_D of the sub-threshold region, the relation between the gate voltages and the surface potential should be known. This relation is stated as Eq (12) where V_{BFB} is the flat-band voltages for BG. C_{BSS}=qN_{BSS} is the capacitance of BG interface traps per unit area, Q_D is a depletion charge density per unit area and ϕ_B is the potential at the BG interfaces. Similarly, the subscript T is used for TG interface. C_S is the capacitance per unit area of a-IGZO semiconductor layer. The detail derivation steps for Eq. (12) are not given in this paper, however it can be found

$$I_D = \frac{W}{L}\frac{\mu}{C_{BI}+C_{TI}}\frac{\{C_{BI}(V_{BG} - V_{BTH0}) + C_{TI}(V_{TG} - V_{TTH0})\}^2}{2}\left[1 - \left\{1 - \frac{(C_{BI}+C_{TI})V_D}{C_{BI}(V_{BG} - V_{BTH0}) + C_{TI}(V_{TG} - V_{TTH0})}\right\}^2\right] \tag{5}$$

$$I_D = \frac{W}{L}\frac{\mu}{C_{BI}+C_{TI}}\frac{\{(C_{BI}+C_{TI})V_G - (C_{BI}V_{BTH0} + C_{TI}V_{TTH0})\}^2}{2}\left[1 - \left\{1 - \frac{(C_{BI}+C_{TI})V_D}{(C_{BI}+C_{TI})V_G - (C_{BI}V_{BTH0} + C_{TI}V_{TTH0})}\right\}^2\right] \tag{6}$$

$$\begin{aligned} V_{BG} + \frac{C_{TI}C_S}{C_{BI}(C_{TI}+C_S+C_{TSS})}V_{TG} &= \left\{\frac{C_{BI}+C_{BSS}}{C_{BI}} + \frac{(C_{TI}+C_{TSS})C_S}{C_{BI}(C_{TI}+C_S+C_{TSS})}\right\}\phi_B - \left\{1 - \frac{C_{TI}+C_{TSS}}{2(C_S+C_{TI}+C_{TSS})}\right\}\frac{Q_D}{C_{BI}} + V_{BFB} \\ &+ \frac{C_{TI}C_S}{C_{BI}(C_{TI}+C_S+C_{TSS})}V_{TFB} \end{aligned} \tag{12}$$

$$\begin{aligned} \left(1 + \frac{C_{TI}C_S}{C_{BI}(C_{TI}+C_S+C_{TSS})}\right)V_G &= \left\{\frac{C_{BI}+C_{BSS}}{C_{BI}} + \frac{(C_{TI}+C_{TSS})C_S}{C_{BI}(C_{TI}+C_S+C_{TSS})}\right\}\phi_B - \left\{1 - \frac{C_{TI}+C_{TSS}}{2(C_S+C_{TI}+C_{TSS})}\right\}\frac{Q_D}{C_{BI}} + V_{BFB} \\ &+ \frac{C_{TI}C_S}{C_{BI}(C_{TI}+C_S+C_{TSS})}V_{TFB} \end{aligned} \tag{13}$$

$$\mathrm{SS} \sim \ln 10 \cdot k_B T \frac{(C_{BI}+C_{BSS})(C_{TI}+C_S+C_{TSS}) + (C_{TI}+C_{TSS})C_S}{C_{BI}(C_{TI}+C_S+C_{TSS}) + C_{TI}C_S} \tag{17}$$

$$\begin{aligned} \left(1 + \frac{C_{TI}(C_{BI}+C_S+C_{BSS})}{C_{BI}C_S}\right)V_G &= \left\{\frac{C_{TI}+C_{TSS}}{C_{BI}} + \frac{(C_{BI}+C_{BSS})(C_{TI}+C_S+C_{TSS})}{C_{BI}C_S}\right\}\phi_T - \left\{1 + \frac{C_{TI}+C_{BSS}}{2C_S}\right\}\frac{Q_D}{C_{BI}} + V_{BFB} \\ &+ \frac{C_{TI}(C_{BI}+C_S+C_{BSS})}{C_{BI}C_S}V_{TFB} \end{aligned} \tag{20}$$

Table 1. Comparison with a conventional TFT Model

	Conventional TFT (Single Gate)	Dual Gate TFT (V_G=V_{BG}=V_{TG})
I_D (Lin.) – Eq. (10)	$I_D = \frac{W}{L}\mu C_G(V_G - V_{TH})V_D$	$I_D = \frac{W}{L}\mu C_{DI}(V_G - V_{DTH})V_D$
I_D (Sat.) – Eq. (11)	$I_D = \frac{W}{2L}\mu C_G(V_G - V_{TH})^2$	$I_D = \frac{W}{2L}\mu C_{DI}(V_G - V_{DTH})^2$
SS – Eq. (23)	$\ln 10 \cdot k_B T\left(1 + \frac{C_{BSS} + C_{TSS}}{C_G}\right)$	$\ln 10 \cdot k_B T\left(1 + \frac{C_{BSS} + C_{TSS}}{C_{DI}}\right)$
Mobility (Lin.)	μ	μ
Mobility (Sat.)	μ	μ
Gate Capacitance	C_G	$C_{DI} = C_{BI} + C_{TI}$
Threshold Voltage	V_{TH}	$V_{DTH} = \frac{C_{BI}V_{BTH0} + C_{TI}V_{TTH0}}{C_{DI}}$

in [9].

Since V_G=V_{BG}=V_{TG} in synchronized DG operation, Eq (12) is reduced as Eq. (13).

When I_D mainly flows near the bottom interface, I_D is given by [12]

$$I_D \sim \mu \frac{W}{L} k_B T \left(1 - e^{-V_D/k_B T}\right) t_{B\_eff} e^{\phi_B/k_B T} \quad (14)$$

From the definition of SS

$$SS \equiv \frac{\partial V_G}{\partial \log(I_D)} \quad (15)$$

Substitution of Eq. (14) into Eq. (15) gives

$$SS \sim \ln 10 \cdot k_B T \left(\frac{\partial \phi_B}{\partial V_G}\right)^{-1} \quad (16)$$

Then, Eq (17) is obtained. If the C_S is larger than other capacitances, $C_s \gg C_{TI}, C_{BI}, C_{TSS}, C_{BSS}$

$$SS \sim \ln 10 \cdot k_B T \left(1 + \frac{C_{BSS} + C_{TSS}}{C_{DI}}\right) \quad (18)$$

If I_D mainly flows near the top interface, SS is given by

$$I_D \sim \mu \frac{W}{L} k_B T \left(1 - e^{-V_D/k_B T}\right) t_{T\_eff} e^{\phi_T/k_B T} \quad (19)$$

and Eq. (20) is given from [9]. Again,

$$SS \sim \ln 10 \cdot k_B T \left(\frac{\partial \phi_T}{\partial V_G}\right)^{-1} \quad (21)$$

$$\sim \ln 10 \cdot k_B T \left(1 + \frac{C_{BSS} + C_{TSS}}{C_{DI}}\right) \quad (22)$$

Hence, we have SS for of DG TFTs when V_G=V_{BG}=V_{TG}:

$$SS = \ln 10 \cdot k_B T \left(1 + \frac{C_{BSS} + C_{TSS}}{C_{DI}}\right) \quad (23)$$

The value of $\ln 10 \cdot k_B T$, which is the smallest value of SS, is about 60 mV at room temperature.

Comparison with a conventional TFT model

For the comparison with the model of the conventional single gate TFTs, the equations derived in previous sections are summarized in Table. 1. Table 1implies that, when V_G=V_{BG}=V_{TG}, the DG TFTs can be considered as the conventional TFTs with the gate capacitance of $C_{DI} = C_{BI} + C_{TI}$ and the threshold voltage of $V_{DTH} = (C_{BI}V_{BTH0} + C_{TI}V_{TTH0})/C_{DI}$. Otherwise, the mobility and the density of interface trap states (N_{TSS} and N_{BSS}) are supposed to be same as the values of the conventional TFTs.

In order to confirm the validity of the models, the TFT parameters of the fabricated DG coplanar homojunction a-IGZO TFT are extracted using the derived models. (Table 2) The schematic cross-section of the fabricated TFTs is illustrated in Figure 2. The bottom gate insulator has 200 nm thickness of silicon oxide and the top gate insulator has a tri-insulator structure, a-SiOx/a-SiNx/a-SiOx. The thickness of tri-layer is 150/300/50 nm, respectively. The capacitance of the tri-layer is calculated using three serially connected capacitors. The values of C_{BI}, C_{TI}, and C_S are 17.7, 9.7, and 295 nF/cm^2. The dielectric constants for a-SiOx and a-SiNx are $3 \cdot \varepsilon_0$ and $7 \cdot \varepsilon_0$, respectively, where ε_0 is the dielectric constant for the air. The channel length (L) is 10 μm. It is assumed that the BG and TG interface trap capacitances are same (C_{BSS}=C_{TSS}) for convenience. i.e. N_{SS}=N_{TSS}=N_{BSS}.

The measured transfer characteristics are shown in Figure 3. The best linear fit to Eq (10) and (11) from 10% to 90%

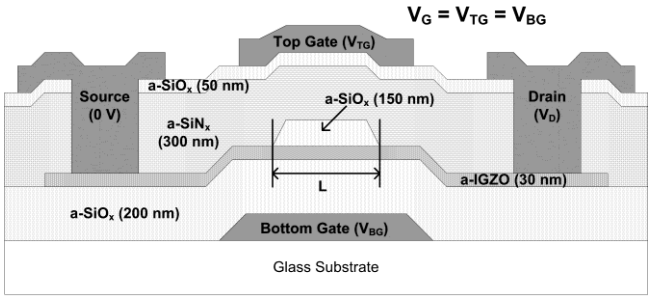

Figure 2. Schematic cross-section of a fabricated DG coplanar homojunction a-IGZO TFT

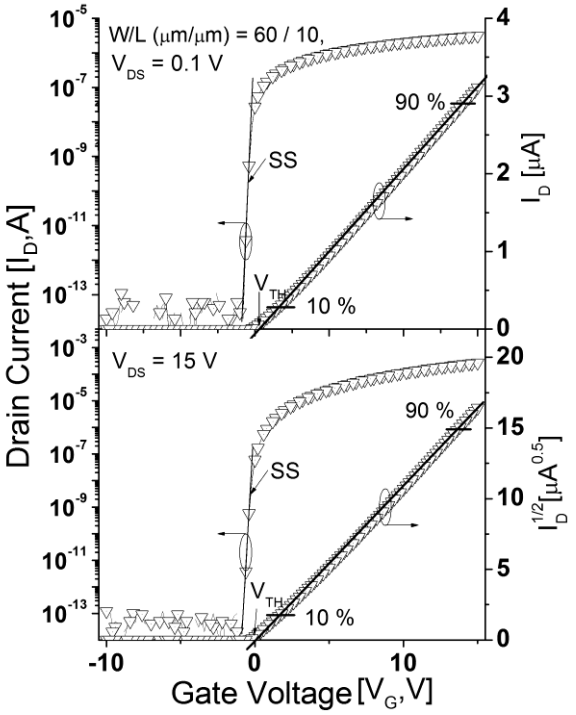

Figure 3. Transfer characteristics of a synchronized DG a-IGZO TFT (top) in linear region (V_{DS} = 0.1V) (bottom) in saturation region (V_{DS} = 15V)

of the maximum I_D is used for the extraction. The μ and N_{SS} for single gate coplanar homojuction a-IGZO TFTs were previously reported as 12.4 $cm^2/V{\cdot}s$ and 7.3×10^{10} $eV^{-1}cm^{-2}$, respectively.[9] From the Table 2, we can find that the extracted μ and N_{SS} are comparable to the previously reported values.

Table 2. Extracted TFT parameters of the synchronized DG a-IGZO TFT

Parameters	Values
V_{DTH} [V]	0.55
μ (Lin) [$cm^2/V{\cdot}s$]	13.08
μ (Sat) [$cm^2/V{\cdot}s$]	15.07
SS [mV/dec]	100
C_{DI} [nF/cm^2]	27.2 (= 9.7+17.7)
N_{SS} [$eV^{-1}cm^{-2}$]	5.8×10^{10}

Summary

The electrical characteristics of DG a-IGZO TFTs with an analytical model for synchronized gate bias are developed. We conclude that the DG TFTs under the bias condition of V_G=V_{BG}=V_{TG} can be simply considered as the conventional TFTs with the gate capacitance of $C_{DI} = C_{BI} + C_{TI}$ and the threshold voltage of $V_{DTH} = (C_{BI}V_{BTH0} + C_{TI}V_{TTH0})/C_{DI}$. The extracted mobility and N_{SS} are consistent with those of the conventional TFTs. This consistency suggests that the calculated models can successfully explain the electrical behaviors of the DG a-IGZO TFTs.

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